ABSTRACT OF THE DISCLOSURE

A split gate flash memory cell. The memory cell includes a substrate, a conductive stud, source/drain regions, an insulating layer, a conductive spacer, an insulating stud, a first conductive layer, and a first insulating spacer. The conductive stud is disposed in the lower trench of the substrate. The source region is formed in the substrate adjacent to the upper conductive stud having the insulating layer thereon. The conductive spacer is disposed on the upper sidewall of the trench serving as a floating gate. The insulating stud is disposed on the insulating layer. The first conductive layer is disposed over the substrate of the outside conductive spacer serving as a control gate. The first insulating spacer is disposed on the sidewall of the insulating stud to cover the first conductive layer. The drain region is formed in the substrate of the outside first conductive layer.